

## Formal Verification An Essential Toolkit For Modern Vlsi Design

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### **Formal Verification - O'Reilly Media**

Formal verification techniques are a relatively new paradigm for equivalence checking. Instead of input stimuli, these techniques perform exhaustive proof through rigorous logical reasoning. The primary approaches used for formal verification include binary decision diagrams (BDDs) and Boolean satisfiability (SAT) [Velev 2001].

### **Design Verification - an overview | ScienceDirect Topics**

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